REMARKS

Applicant has reviewed the comments, objections, and rejections set forth by the Examiner in the Office Action dated April 6, 2005 and respectfully respond with the amendments above and the following remarks. Claims 1-3, 7-12, and 17-21 are pending in the present case. Independent Claims 1, 17 and 20 are amended herein. Applicant respectfully requests reconsideration in view of the above amendments and the arguments set forth below.

ALLOWABLE SUBJECT MATTER

Attorney for Applicant has telephonically conferred with the Examiner on July 1, 2005 and July 5, 2005 to discuss the instant Office Action of April 6, 2005 in the context of the previous Office Actions dated April 7, 2003, wherein Claims 14-19 were ALLOWED, and the Office Actions dated September 26, 2003, April 26, 2004 and October 15, 2004, wherein various subject matter was indicated to be ALLOWABLE.

Applicant respectfully notes that the respective responses to the Office Actions dated September 26, 2003, April 26, 2004 and October 15, 2004 included claim amendments wherein Applicant respectfully incorporated the subject matter that the Examiner had indicated to be allowable.

Applicant respectfully and regretfully notes that the Examiner has withdrawn ALL allowed claims and allowable subject matter granted in the previous Office Actions listed.

OBJECTIONS TO THE SPECIFICATION

The specification is objected to for informality. Applicant has reviewed the specification in the place cited (the paragraph begins on line 21 at page 7 and continues through line 2 at page 9) and respectfully disagrees with the Examiner that the equation cited (appearing between lines 6 and 9 at page 8),

$$VPP1 = VREF ((C1 + C2A)/C1)$$

is misleading. Applicant respectfully assets that VPP is thus regulated, e.g., that VPPDiv1, the voltage corresponding to the ratio between capacitors C1 and C2, is compared with comparator 118 to generate VPPComp1, with which VPP is indeed regulated, as clearly depicted in Figure 1 (amended by Replacement Sheet submitted with the January 26, 2004 response to the Office Action dated September 26, 2003) by comparator 118. The Examiner's review and approval is respectfully elicited.

CLAIM REJECTIONS

REJECTIONS UNDER 35 USC 112

Claims 17-21 are rejected under 35 USC 112. Claim 17 and 20 are amended herein to comport with the statute, in response to the Examiner's comments. As amended herein, Claims 1 and 20 read as follows, with underlining added for emphasis:

> 17. A switched capacitor controller for controlling a rise time of an on-chip generated voltage source, comprising:
> a charge pump for converting an input voltage corresponding to said signal to an output voltage greater than said input voltage;
> a ramp generator coupled to said charge pump, wherein said ramp generator comprises a switched capacitor network;

a regulator circuit coupled to said switched capacitor network which causes a capacitor to switch between ground potential and the potential at a node, wherein a stair-step ramp signal is generated and said rise time is controlled with said switched capacitor and wherein said switched capacitor network comprises two capacitors wherein said rise time is controlled according to a ratio of capacitances of said two capacitors; and

an oscillator coupled to said charge pump which generates an oscillating signal to said charge pump; and

a keeper device coupled to said charge pump for selectively allowing said charge pump to hold said signal at said supply voltage and, upon enabling, to perform said converting.

20. In a flash memory, a method for controlling a rise time of an on-chip generated voltage source used to program said flash memory, comprising:
generating a programming voltage VPP for programming a cell of flash memory from a power supply via a ring oscillator, wherein said programming voltage is selectively greater than a supply voltage VCC from said power supply upon enabling and held to said supply voltage VCC without said enabling;
activating a program control signal PGM to enable programming of said cell of said flash memory;

generating a stair-case ramp corresponding to said programming voltage VPP in response to said program control signal PGM, wherein steps of said stair-case ramp have a period corresponding to a clock signal generated by a clock generator and voltage increases corresponding to a reference voltage times a ratio of two capacitor values.

As amended herein, independent Claims 17 and 20 have been corrected, and various signals recited in Claim 20 have been clarified in accordance with the Examiner's comments. No new matter is added herein. As explained above, VPP is regulated, e.g., VPPDiv1, the voltage corresponding to the ratio between

capacitors C1 and C2, is compared with comparator 118 to generate VPPComp1, with which VPP is indeed regulated by comparator 118.

Applicant respectfully asserts that, as amended herein, independent Claims 17 and 20 and their respective dependent claims are definite. Thus, Applicant respectfully asserts that Claims 17-21 are allowable under 35 USC 112 (second paragraph).

REJECTIONS UNDER 35 USC 102

Claims 1-3, 7-8, 10-12 and 17-21 are rejected under 35 USC 102(e) as anticipated by US Patent No. 5,168,174 to Naso, et al. (hereinafter Naso). Applicant respectfully notes that the Naso reference was cited in the previous Office Action dated September 26, 2003 and overcome in Applicant's response thereto dated January 26, 2004, with the incorporation of subject matter then indicated by the Examiner to be allowable. Applicants have again reviewed the reference cited and respectfully assert it does not anticipate the embodiments of the present invention as recited in Claims 1-3, 7-8, 10-12 and 17-21 for the following rationale.

As Applicants understand the reference, Naso teaches a negative voltage charge pump with feedback control. Naso, col. 1, ll. 64-66. Claims 1-3, 7-8, 10-12 and 17-21 differ from the teachings of Naso. As amended herein, independent Claims 1, 17 and 20 are to read as shown below, with underlining added herein for emphasis.

> 1. A circuit for controlling the rise time of a signal, comprising:
>
> a voltage multiplication circuit for converting an input voltage corresponding to said signal to an output voltage greater than said input voltage;

a ramp generator coupled to said voltage multiplication circuit for controlling said output voltage from said voltage multiplication circuit, wherein a ratio between a first capacitor of said ramp generator and a second capacitor of said ramp generator determines said rise time of said signal, wherein said signal comprises a staircase ramp signal;

a divide by N counter coupled to said ramp generator for generating a plurality of clock phases wherein said ramp generator is controlled with said clock phases; and

a keeper device coupled to said voltage multiplication circuit for allowing said voltage multiplication circuit to selectively hold said signal at said supply voltage and, upon enabling, to perform said converting.

17. A switched capacitor controller for controlling a rise time of an on-chip generated voltage source, comprising:

a charge pump for converting an input voltage corresponding to said signal to an output voltage greater than said input voltage;

a ramp generator coupled to said charge pump, wherein said ramp generator comprises a switched capacitor network;

a regulator circuit coupled to said switched capacitor network which causes a capacitor to switch between ground potential and the potential at a node, wherein a stair-step ramp signal is generated and said rise time is controlled with said switched capacitor and wherein said switched capacitor network comprises two capacitors wherein said rise time is controlled according to a ratio of capacitances of said two capacitors; and

an oscillator coupled to said charge pump which generates an oscillating signal to said charge pump; and

a keeper device coupled to said charge pump for selectively allowing said charge pump to hold said signal at said supply voltage and, upon enabling, to perform said converting.

20. In a flash memory, a method for controlling a rise time of an on-chip generated voltage source used to program said flash memory, comprising:

generating a programming voltage VPP for programming a cell of flash memory from a power supply via a ring oscillator, wherein said programming voltage is selectively greater than a supply voltage VCC from said power supply upon enabling and held to said supply voltage VCC without said enabling;

activating a program control signal PGM to enable programming of said cell of said flash memory;

generating a stair-case ramp corresponding to said programming voltage VPP in response to said program control signal PGM, wherein steps of said stair-case ramp have a period corresponding to a clock signal generated by a clock generator and voltage increases corresponding to a reference voltage times a ratio of two capacitor values.

As amended herein, Claims 1 and 17 respectively recite a circuit and a controller that include a keeper device for selectively allowing a voltage multiplier, a charge pump, etc. to selectively hold programming voltage at a level corresponding to the supply voltage level absent enabling, and upon enabling, to convert the supply voltage to the higher programming voltage. Further, Claim 20 is amended herein after a similar fashion, recited in terms of the method claimed therein. This has the benefit of providing control, thus allowing VPP to be pumped by the charge pump, voltage multiplier, etc., upon the enabling signal therefor going high.

Applicant finds no teaching or suggestion in Naso directed towards such a keeper device or a related functionality. Moreover, Naso expressly teaches that "When the charge pump circuit is disabled [in contrast to 'enabled'], ... the output voltage is forced to a constant reference positive voltage." Naso, col. 4, ll. 37-40. Applicant respectfully asserts therefore that the cited Naso reference expressly teaches away from the embodiments recited in Claims 1, 17 and 20 and their

respective dependent claims, wherein VPP is held to VCC when the charging pump, voltage multiplier, etc. is disabled.

Thus, Applicant respectfully asserts that Naso does not teach or suggest the embodiments recited in Claims 1, 17 and 20 and their respective dependent claims (i.e., Claims 1-3, 7-8, 10-12 and 17-21), which relate to a keeper device for selectively allowing a voltage multiplier, a charge pump, etc. to selectively hold programming voltage at a level corresponding to the supply voltage level absent enabling, and upon enabling, to convert the supply voltage to the higher programming voltage. In fact, Applicant respectfully reiterates his respectful assertion that the reference in fact expressly teaches away therefrom.

REJECTIONS UNDER 35 USC 103

Claim 9 is rejected under 35 USC 103(a) over Naso in view of US Patent No. 6,492,862 to Nakahara (hereinafter Nakahara). Applicant respectfully re-asserts each and every point above made relating to the Naso reference. More specifically, Applicant respectfully re-asserts that Naso does not teach or suggest the embodiments recited in Claim 1 and its dependent Claims, including Claim 9, and in fact expressly teaches away therefrom. Applicant also finds no motivation in Naso to modify its teachings per Nakahara to obtain the embodiments recited herein. Applicant finds no teaching, suggestion, or motivation in Nakahara that corrects this defect of Naso.

Applicant understands Nakahara to teach a charge pump voltage conversion circuit generating a boosted output voltage with reduced ripple. Nakahara, col. 1, ll. 17-11; col. 4, l. 61-col. 5, l. 11. However, Applicant finds no teaching or suggestion in Nakahara directed towards a circuit and a controller that include a keeper device for

selectively allowing a voltage multiplier, a charge pump, etc. to selectively hold programming voltage at a level corresponding to the supply voltage level absent enabling, and upon enabling, to convert the supply voltage to the higher programming voltage, as recited in independent Claim 1 herein and its dependent Claim 9. Applicant also finds no motivation therein for combining its teaching with Naso's to obtain the recited embodiments herein. Moreover, Applicant finds no teaching, suggestion or motivation in Naso that cures this defect of Nakahara.

Applicant respectfully points out that, obviousness can only be established by combining or modifying the teachings of the references cited to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found in either the references themselves or knowledge generally available to one of ordinary skill in the art. MPEP § 2143.01; In re Fine, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988); In re Jones, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). Here, Applicant finds no such teaching, suggestion or motivation in either reference to combine its teachings with those of the other to achieve the embodiments recited herein.

Thus, Applicant respectfully asserts that Claim 9 is allowable over Naso in view of Nakahara under 35 USC 103(a).

CONCLUSION

By the rationale stated above, Applicant respectfully asserts that the specification is free of informalities. Accordingly, Applicant respectfully requests that the objection to the specification be withdrawn and that the specification be approved.

By the rationale stated above, Applicant respectfully asserts that Claims 17-21 comply with 35 USC 112 (¶2), that Claims 1-3, 7-8, 10-12 and 17-22 are allowable over Naso under 35 USC 102(e) and that Claim 9 is allowable over Naso in view of Nakahara under 35 USC 103(a). Accordingly, Applicant respectfully requests that the rejections of Claims 17-21 under 35 USC 112 (¶2), of Claims 1-3, 7-8, 10-12 and 17-22 under 35 USC 102(e) and Claim 9 under 35 USC 103(a) be withdrawn and that Claims 1-3, 7-12 and 17-21 be allowed.

Please charge our deposit account No. 23-0085, for any unpaid fees.

Respectfully submitted,

WAGNER, MURABITO & HAO, LLP

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Lawrence R. Goerke
Reg. No. 45,927

WAGNER, MURABITO & HAO, LLP
Two North Market Street, Third Floor
San Jose, CA 95113

Tel.: (408) 938-9060
Fax: (408) 938-9069